Engr354 **Digital Logic** **Autumn 2019**

Text: Fundamentals of Digital Logic with VHDL Design, 3rd Edition Brown and Vranesic, 2009

Note: Schedule subject to change with appropriate notice to students.

Date		Topic	Reading
M	Sep 23	Introduction, Number Systems, Design Process	1.1-6, Notes
W	25	Terminology, Gates, Truth Tables, Boolean Algebra	2.1-5
F	27	Boolean Algebra, DeMorgan's Laws, Synthesis	2.5,6
M	30	Synthesis, Examples **(1:35)**	2.6-8
W	Oct 2	Logic Minimization, K-Maps **(1:35)**	4.1-4
F	4	K-Maps, Don't Cares, Entered Variable Maps **(1:35)**	4.1-4, Notes
M	7	Entered Variable Minimization	Notes
W	9	Logic Board Construction. Implementation Technology	Notes, 3.1-6
F	11	Logic Board Construction, Multiplexers	Notes, 6.1
M	14	Logic Board Debugging, Multiplexers	Notes, 6.1
W	**16**	**Service Day – No Class**	
F	18	Combinational Devices, Decoders and Demultiplexers	6.2-3
M	21	Code Converters, Arithmetic Circuits	6.4,5.1-6
W	23	Arithmetic Circuits, Midterm Review	5.1-6, Notes
F	**25**	**Mid-term Exam #1**	**Chaps 1-6**
M	28	Synchronous Systems: Models, Basic Memory	7.1-2, Notes
W	30	Latches	7.3
F	Nov 1	Flip-Flops	7.4-7
M	4	State Machines: Models, State Diagrams	8.1-3
W	6	State Machine Design Examples	8.1-3
F	8	State Machine Design Examples	8.1-3
M	11	Alternative State Machine Architectures	Notes
W	13	Registers and Counters, Class Project Discussion	7.8-11
F	15	Class Project Discussion, Test Review	
M	**18**	**Mid-term Exam #2**	**Chaps 7,8**
W	20	Video – Silicon Run I	
F	22	No Class	
M	25	Thanksgiving Vacation	
W	28	" "	
F	30	" "	
M	Dec 2	Project Work; VHDL Synthesis	Notes
W	4	Project Work	
F	6	Course Summary and Evaluation	Project Checkout
T	**10**	**Final Exam Time (10am – noon)**	